Jameco Part number 157307

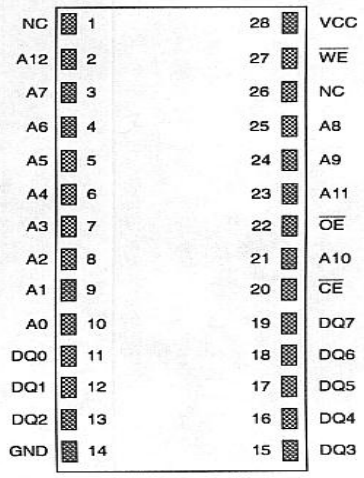
DALLAS SEMICONDUCTOR

DS1225AB/AD
64K Nonvolatile SRAM

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 8K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low–power CMOS
- JEDEC standard 28–pin DIP package
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full ±10% V_{CC} operating range (DS1225AD)
- Optional ±5% V_{CC} operating range (DS1225AB)
- Optional industrial temperature range of –40°C to +85°C, designated IND

PIN ASSIGNMENT



28–PIN ENCAPSULATED PACKAGE
720 MIL EXTENDED

PIN ASSIGNMENT

PIN DESCRIPTION

A0-A12	- Address Inputs
DQ0-DQ7	- Data In/Data Out
CE	- Chip Enable
WE	- Write Enable
OE	- Output Enable
Vcc	- Power (+5V)
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS1225AB and DS1225AD are 65,536-bit, fully static, nonvolatile SRAMs organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors Vcc for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAMs can be used in place of existing 8K x 8 SRAMs directly conforming to the popular bytewide 28-pin DIP standard. The devices also match the pinout of the 2764 EPROM and the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

READ MODE

The DS1225AB and DS1225AD execute a read cycle whenever WE (Write Enable) is inactive (high) and CE (Chip Enable) and OE (Output Enable) are active (low). The unique address specified by the 13 address inputs (A_0-A_{12}) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE and OE access times are also satisfied. If CE and OE access times are not satisfied, then data access must be measured from the later occurring signal and the limiting parameter is either t_{CO} for CE or t_{OE} for OE rather than address access.

WRITE MODE

The DS1225AB and DS1225AD execute a write cycle whenever the WE and CE signals are active (low) after address inputs are stable. The latter occurring falling edge of CE or WE will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE or WE. All address inputs must be kept valid throughout the write cycle. WE must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled (CE and OE active) then WE will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1225AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1225AD provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1225AB and 4.5 volts for the DS1225AD.

FRESHNESS SEAL

Each DS1225 is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than V_{TP} the lithium energy source is enabled for battery backup operation.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1225AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1225AD Power Supply Voltage	V_{CC}	4.50	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

(V_{CC}=5V ± 5% for DS1225AB)

DC ELECTRICAL CHARACTERISTICS (t_A: See Note 10) (V_{CC}=5V ± 10% for DS1225AD)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current CE>V_{IH} <V_{CC}	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current CE = 2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current CE = V_{CC}-0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC}=200 ns (Commercial)	I_{CC01}			75	mA	
Operating Current t_{CYC}=200 ns (Industrial)	I_{CC01}			85	mA	
Write Protection Voltage (DS1225AB)	V_{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1225AD)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE (t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

(V_{CC}=5V ± 5% for DS1225AB)

AC ELECTRICAL CHARACTERISTICS ($t_{A:}$ See Note 10) (V_{CC}=5V ± 10% for DS1225AD)

PARAMETER	SYMBOL	DS1225AB=70 DS1225AD-70		DS1225AB=85 DS1225AD-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		85		ns	
Access Time	t_{ACC}		70		85	ns	
OE to Output Valid	t_{OE}		35		45	ns	
CE to Output Valid	t_{CO}		70		85	ns	
OE or CE to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		30	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write Pulse Width	t_{WP}	55		65		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1}	0		0		ns	12
	t_{WR2}	10		10		ns	13
Output High Z from WE	t_{ODW}		25		30	ns	5
Output Active from WE	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		35		ns	4
Data Hold Time	t_{DH1}	0		0		ns	12
	t_{DH2}	10		10		ns	13

PARAMETER	SYMBOL	DS1225AB=150 DS1225AD=150		DS1225AB=200 DS1225AD=200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
OE to Output Valid	t_{OE}		70		100	ns	
CE to Output Valid	t_{CO}		150		200	ns	
OE or CE to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		35		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	100		100		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1}	0		0		ns	12
	t_{WR2}	10		10		ns	13
Output High Z from ??WE	t_{ODW}		35		35	ns	5
Output Active from ??WE	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH1}	0		0		ns	12
	t_{DH2}	10		10		ns	13

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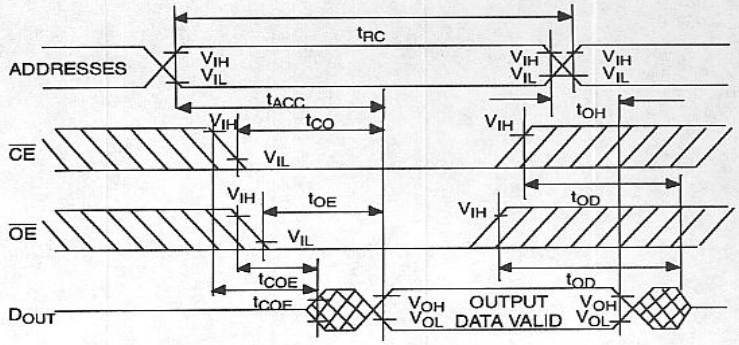
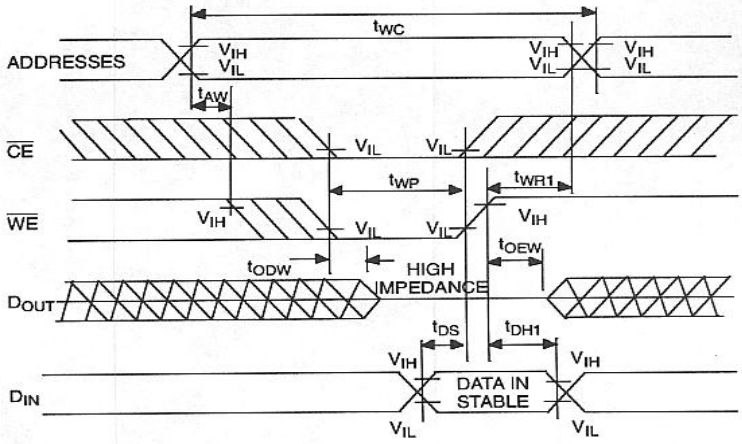
READ CYCLE



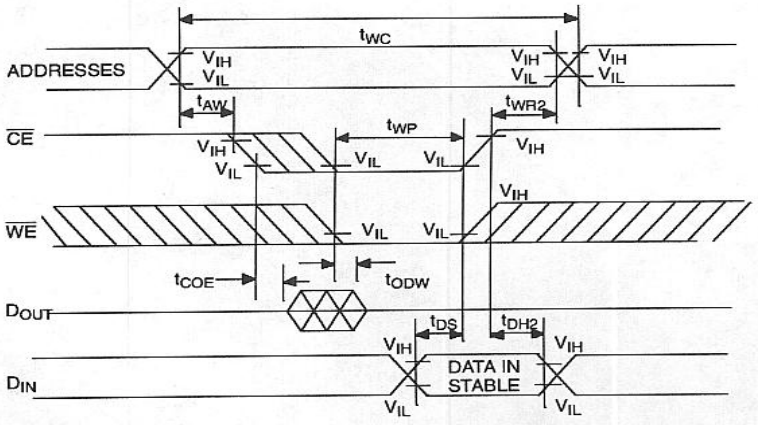
SEE NOTE 1

WRITE CYCLE 1



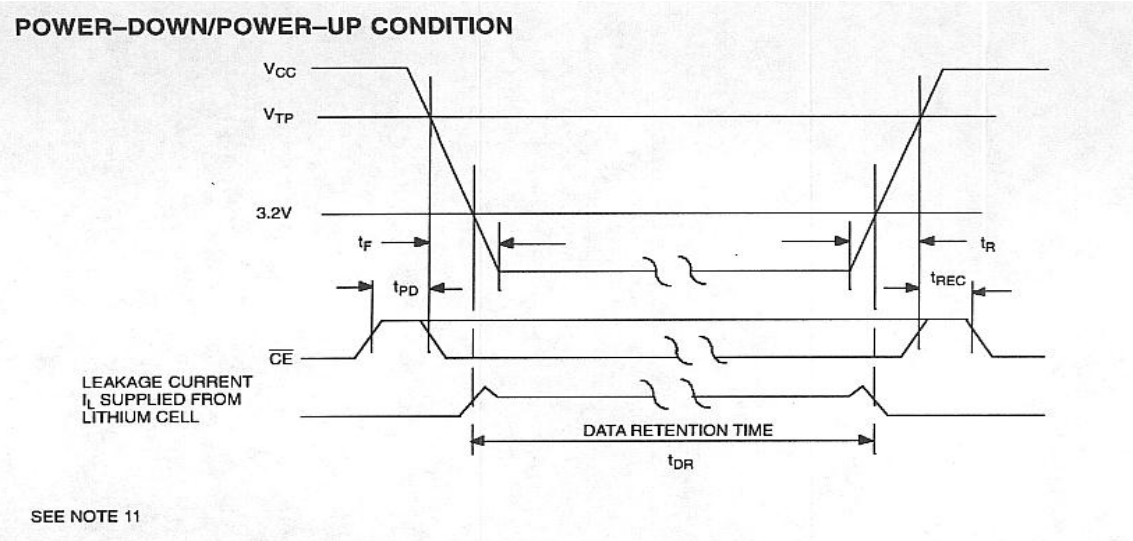
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING (t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{cc} Slew from V_{TP} to 0V	t_F	300			µs	
V_{cc} Slew from 0V to V_{TP}	t_R	300			µs	
CE at V_{IH} after Power-Up	t_{REC}	2		125	ms	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

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NOTES:

1. WE is high for a read cycle.
2. OE = V_{IH} or V_{IL}. If OE = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of CE and WE. t_{WP} is measured from the latter of CE or WE going low to the earlier of CE or WE going high.
4. t_{DS} are measured from the earlier of CE or WE going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the CE low transition occurs simultaneously with or later than the WE low transition, the output buffers remain in a high impedance state during this period.
7. If the CE high transition occurs prior to or simultaneously with the WE high transition, the output buffers remain in a high impedance state during this period.
8. If WE is low or the WE low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1225AB and each DS1225AD has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from WE going high.
13. t_{WR2}, t_{DH2} are measured from CE going high.
14. DS1225AB and DS1225AD modules are recognized by Underwriters Laboratory (U.L.(R)) under file E99151.

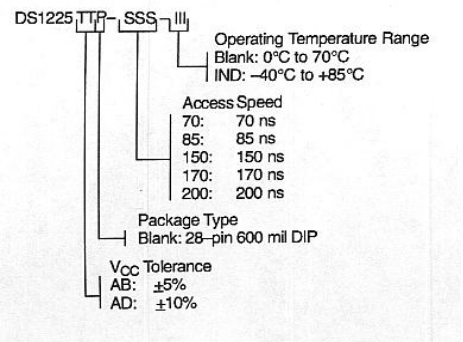
DC TEST CONDITIONS

Outputs Open
All Voltages Are Referenced to Ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

ORDERING INFORMATION



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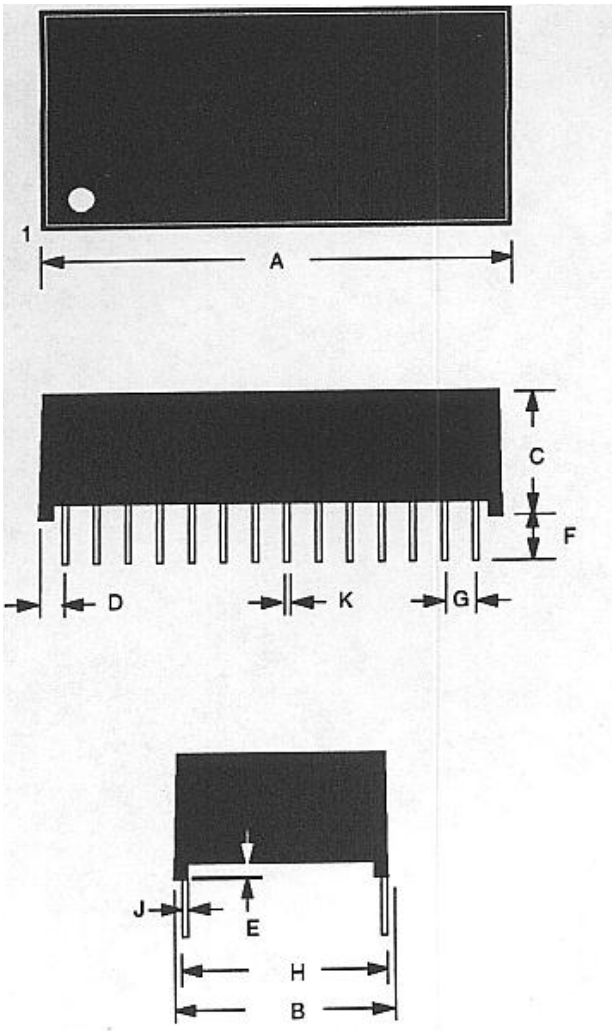
DS1225AB/AD NONVOLATILE SRAM, 28-PIN 720 MIL EXTENDED MODULE



PKG	28–PIN	
DIM	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53